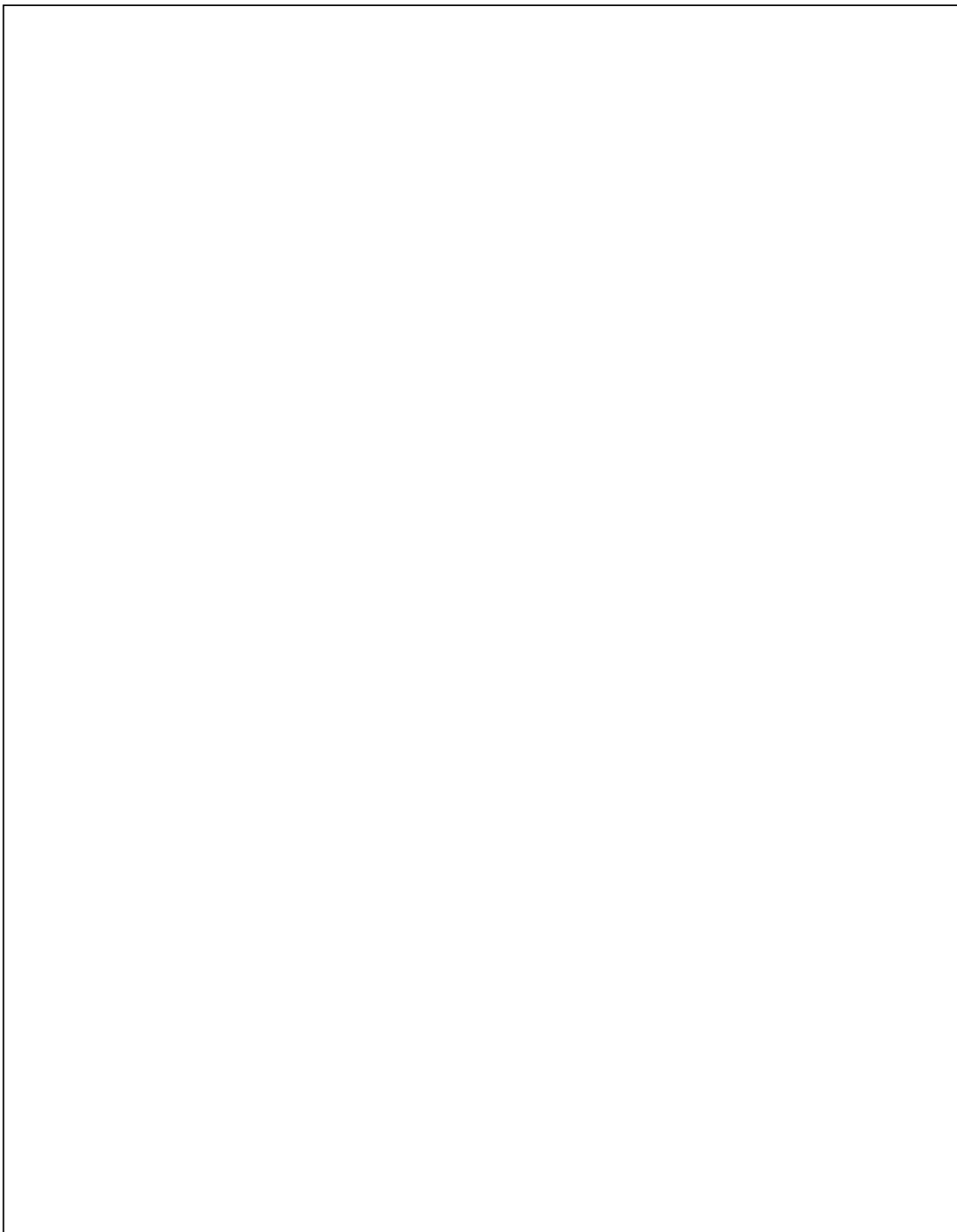


[]



9

9.1 MC

(MC→PLC) :

MC

PLC

9.1 MC

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
I00			DNC	MPG	STP	JOG	ORG	AUT	AZP	OP	SPL	STL	AL	RST	SA	MA
I01	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	ZP8	ZP7	ZP6	ZP5	ZP4	ZP3	ZP2	ZP1
I02	M28	M24	M22	M21	M18	M14	M12	M11	MF					M02		
I03	AA8	AA7	AA6	AA5	AA4	AA3	AA2	AA1	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1
I04	-L8	+L8	-L7	+L7	-L6	+L6	-L5	+L5	-L4	+L4	-L3	+L3	-L2	+L2	-L1	+L1
I05	PI1F	PI1E	PI1D	PI1C	PI1B	PI1A	PI19	PI18	PI17	PI16	PI15	PI14	PI13	PI12	PI11	PI10
I06	Ph1F	Ph1E	Ph1D	Ph1C	Ph1B	Ph1A	Ph19	Ph18	Ph17	Ph16	Ph15	Ph14	Ph13	Ph12	Ph11	Ph10
I07	PI2F	PI2E	PI2D	PI2C	PI2B	PI2A	PI29	PI28	PI27	PI26	PI25	PI24	PI23	PI22	PI21	PI20
I08	Ph2F	Ph2E	Ph2D	Ph2C	Ph2B	Ph2A	Ph29	Ph28	Ph27	Ph26	Ph25	Ph24	Ph23	Ph22	Ph21	Ph20
I09	PI3F	PI3E	PI3D	PI3C	PI3B	PI3A	PI39	PI38	PI37	PI36	PI35	PI34	PI33	PI32	PI31	PI30
I10	Ph3F	Ph3E	Ph3D	Ph3C	Ph3B	Ph3A	Ph39	Ph38	Ph37	Ph36	Ph35	Ph34	Ph33	Ph32	Ph31	Ph30
I11	PI4F	PI4E	PI4D	PI4C	PI4B	PI4A	PI49	PI48	PI47	PI46	PI45	PI44	PI43	PI42	PI41	PI40
I12	Ph4F	Ph4E	Ph4D	Ph4C	Ph4B	Ph4A	Ph49	Ph48	Ph47	Ph46	Ph45	Ph44	Ph43	Ph42	Ph41	Ph40
I13	PI5F	PI5E	PI5D	PI5C	PI5B	PI5A	PI59	PI58	PI57	PI56	PI55	PI54	PI53	PI52	PI51	PI50
I14	Ph5F	Ph5E	Ph5D	Ph5C	Ph5B	Ph5A	Ph59	Ph58	Ph57	Ph56	Ph55	Ph54	Ph53	Ph52	Ph51	Ph50
I15	PI6F	PI6E	PI6D	PI6C	PI6B	PI6A	PI69	PI68	PI67	PI66	PI65	PI64	PI63	PI62	PI61	PI60
I16	Ph6F	Ph6E	Ph6D	Ph6C	Ph6B	Ph6A	Ph69	Ph68	Ph67	Ph66	Ph65	Ph64	Ph63	Ph62	Ph61	Ph60
I17	PI7F	PI7E	PI7D	PI7C	PI7B	PI7A	PI79	PI78	PI77	PI76	PI75	PI74	PI73	PI72	PI71	PI70
I18	Ph7F	Ph7E	Ph7D	Ph7C	Ph7B	Ph7A	Ph79	Ph78	Ph77	Ph76	Ph75	Ph74	Ph73	Ph72	Ph71	Ph70
I19	PI8F	PI8E	PI8D	PI8C	PI8B	PI8A	PI89	PI88	PI87	PI86	PI85	PI84	PI83	PI82	PI81	PI80
I20	Ph8F	Ph8E	Ph8D	Ph8C	Ph8B	Ph8A	Ph89	Ph88	Ph87	Ph86	Ph85	Ph84	Ph83	Ph82	Ph81	Ph80
I21	FIF	FIE	FID	FIC	FIB	FIA	FI9	FI8	FI7	FI6	FI5	FI4	FI3	FI2	FI1	FI0
I22	FhF	FhE	FhD	FhC	FhB	FhA	Fh9	Fh8	Fh7	Fh6	Fh5	Fh4	Fh3	Fh2	Fh1	Fh0
I23						LE	PE	LrE	P7	P6	P5	P4	P3	P2	P1	P0
I24	AF	AE	AD	AC	AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
I25	CI1F	CI1E	CI1D	CI1C	CI1B	CI1A	CI19	CI18	CI17	CI16	CI15	CI14	CI13	CI12	CI11	CI10
I26	Ch1F	Ch1E	Ch1D	Ch1C	Ch1B	Ch1A	Ch19	Ch18	Ch17	Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10
I27	CI2F	CI2E	CI2D	CI2C	CI2B	CI2A	CI29	CI28	CI27	CI26	CI25	CI24	CI23	CI22	CI21	CI20
I28	Ch2F	Ch2E	Ch2D	Ch2C	Ch2B	Ch2A	Ch29	Ch28	Ch27	Ch26	Ch25	Ch24	Ch23	Ch22	Ch21	Ch20
I29	CI3F	CI3E	CI3D	CI3C	CI3B	CI3A	CI39	CI38	CI37	CI36	CI35	CI34	CI33	CI32	CI31	CI30
I30	Ch3F	Ch3E	Ch3D	Ch3C	Ch3B	Ch3A	Ch39	Ch38	Ch37	Ch36	Ch35	Ch34	Ch33	Ch32	Ch31	Ch30
I31	CI4F	CI4E	CI4D	CI4C	CI4B	CI4A	CI49	CI48	CI47	CI46	CI45	CI44	CI43	CI42	CI41	CI40
I32	Ch4F	Ch4E	Ch4D	Ch4C	Ch4B	Ch4A	Ch49	Ch48	Ch47	Ch46	Ch45	Ch44	Ch43	Ch42	Ch41	Ch40
I33	CI5F	CI5E	CI5D	CI5C	CI5B	CI5A	CI59	CI58	CI57	CI56	CI55	CI54	CI53	CI52	CI51	CI50
I34	Ch5F	Ch5E	Ch5D	Ch5C	Ch5B	Ch5A	Ch59	Ch58	Ch57	Ch56	Ch55	Ch54	Ch53	Ch52	Ch51	Ch50
I35	CI6F	CI6E	CI6D	CI6C	CI6B	CI6A	CI69	CI68	CI67	CI66	CI65	CI64	CI63	CI62	CI61	CI60
I36	Ch6F	Ch6E	Ch6D	Ch6C	Ch6B	Ch6A	Ch69	Ch68	Ch67	Ch66	Ch65	Ch64	Ch63	Ch62	Ch61	Ch60
I37	CI7F	CI7E	CI7D	CI7C	CI7B	CI7A	CI79	CI78	CI77	CI76	CI75	CI74	CI73	CI72	CI71	CI70
I38	Ch7F	Ch7E	Ch7D	Ch7C	Ch7B	Ch7A	Ch79	Ch78	Ch77	Ch76	Ch75	Ch74	Ch73	Ch72	Ch71	Ch70
I39	CI8F	CI8E	CI8D	CI8C	CI8B	CI8A	CI89	CI88	CI87	CI86	CI85	CI84	CI83	CI82	CI81	CI80
I40	Ch8F	Ch8E	Ch8D	Ch8C	Ch8B	Ch8A	Ch89	Ch88	Ch87	Ch86	Ch85	Ch84	Ch83	Ch82	Ch81	Ch80
I41	LIF	LIE	LID	LIC	LIB	LIA	LI9	LI8	LI7	LI6	LI5	LI4	LI3	LI2	LI1	LI0
I42	LhF	LhE	LhD	LhC	LhB	LhA	Lh9	Lh8	Lh7	Lh6	Lh5	Lh4	Lh3	Lh2	Lh1	Lh0

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
I43	+DI6	Dd5	-DI5	+DI5	Dd4	-DI4	+DI4	Dd3	-DI3	+DI3	Dd2	-DI2	+DI2	Dd1	-DI1	+DI1
I44	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	Dd8	-DI8	+DI8	Dd7	-DI7	+DI7	Dd6	-DI6
I45	EcIF	EcIE	EcID	EcIC	EcIB	EcIA	EcI9	EcI8	EcI7	EcI6	EcI5	EcI4	EcI3	EcI2	EcI1	EcI0
I46	EchF	EchE	EchD	EchC	EchB	EchA	Ech9	Ech8	Ech7	Ech6	Ech5	Ech4	Ech3	Ech2	Ech1	Ech0
I47																
I48																
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1) MA[10.0] ()

MA 가 ON .

2) SA[10.1] SERVO ()

SERVO 가
SERVO ALARM, NOT READY, OVERLOAD SA 가 ON
OFF .

3) RST[10.2] RESET ()

RST KEY, RESET () ERS[00.1] ON RESET OFF .

4) AL[10.3] ALARM ()

ALARM ALARM AL[10.3] ON
ALARM RESET ALARM AL OFF .

5) STL[10.4] ()

SPL[10.5] ()

OP[10.6] ()

		STL [10.4]	SPL [10.5]	OP [10.6]
	AUTO MODE BLOCK .	0	X	0
	AUTO MODE BLOCK .	X	0	0
	AUTO MODE MC RESET .	0	X	0
		x	x	x

26) AZP [10.7] ()

ORG MODE ON .

OFF .

6) AUTO[10.8], ORG[10.9], JOG[10.A], STP[10.B], MPG[10.C], DNC[10.D]

MODE ()

MODE MODE .

7) ZP1[11.0], ZP2[11.1], ZP3[11.2], ZP4[11.3], ZP5[11.4], ZP6[11.5], ZP7[11.6], ZP8[11.7]
()

- ORG MODE , 가 ON .
ORG MODE MODE 가 OFF .

8) MR1[11.8], MR2[11.9], MR3[11.A], MR4[11.B], MR5[11.C], MR6[11.D], MR7[11.E], MR8[11.F]
()

가 ON .

9) M02[/2.2] M02()

M CODE가 ON FIN[00.7] (1) → (0)
 OFF .

10) MF[/2.7] M FUNTION ()

MC M CODE가 ON FIN[00.7] (0) → (1)
 OFF .

11) M11~M28[/2.8~ /2.F] M CODE BCD

M CODE가 BCD CODE FIN[00.7] (1) → (0)
 OFF .

12) DC1[/3.0], DC2[/3.1], DC3[/3.2], DC4[/3.3], DC5[/3.4], DC6[/3.5], DC7[/3.6], DC8[/3.7]
 Switch ()

Switch .

13) AA1[/3.8], AA2[/3.9], AA3[/3.A], AA4[/3.B],
 AA5[/3.C], AA6[/3.D], AA7[/3.E], AA8[/3.F] Alarm ()

Alarm 가 ON .

14) +L1[/4.0], -L1[/4.1], +L2[/4.2], -L2[/4.3], +L3[/4.4], -L3[/4.5], +L4[/4.6], -L4[/4.7],
 +L5[/4.8], -L5[/4.9], +L6[/4.A], -L6[/4.B], +L7[/4.C], -L7[/4.D], +L8[/4.E], -L8[/4.F]
 Limit Switch ()

Limit Switch .

15) PI10 ~ Ph1F[/5, /6]	1	(HEX)
PI20 ~ Ph2F[/7, /8]	2	(HEX)
PI30 ~ Ph3F[/9, /10]	3	(HEX)
PI40 ~ Ph4F[/11, /12]	4	(HEX)
PI50 ~ Ph5F[/13, /14]	5	(HEX)
PI60 ~ Ph6F[/15, /16]	6	(HEX)
PI70 ~ Ph7F[/17, /18]	7	(HEX)
PI80 ~ Ph8F[/19, /20]	8	(HEX)

16) FI0 ~ FhF[/21, /22]

HEX .

17) P0 ~ P7[/23.0~ /23.7]

AUTO MODE HEX .

18) A0 ~ AF[/24]

HEX .

19) LrE[/23.8] L Read End
LI0 ~ LhF[/41, /42] L

PLC → MC LrE(L Read Enable[Q24.A]) L I41, I42 LrE(Data Read End[/23.8])가 ON .

PLC→MC LrE(L Read Enable[Q24.A])가 OFF LrE(Data Read End[/23.8]) OFF .

20) PE[/23.9] ProgEnd

PLC → MC PE([Q24.8])
PE(ProgEnd[/23.9])가 ON .

PLC → MC PE([Q24.8])가 OFF , PE(ProgEnd[/23.9]) OFF .

21) LE[/23.A] L LEnd

PLC → MC LE(L [Q24.9]) L LE(LEnd[/23.A])가 ON .

PLC → MC LE(L [Q24.9])가 OFF , LE(LEnd[/23.A]) OFF .

22)	CI10 ~ Ch1F[/25, /26]	1	(HEX)
	CI20 ~ Ch2F[/27, /28]	2	(HEX)
	CI30 ~ Ch3F[/29, /30]	3	(HEX)
	CI40 ~ Ch4F[/31, /32]	4	(HEX)
	CI50 ~ Ch5F[/33, /34]	5	(HEX)
	CI60 ~ Ch6F[/35, /36]	6	(HEX)
	CI70 ~ Ch7F[/37, /38]	7	(HEX)
	CI80 ~ Ch8F[/39, /40]	8	(HEX)

23) LI0 ~ LhF[/41, /42] L (LrE[/23.8])

23)

+DI1[/43.0], +DI2[/43.3], +DI3[/43.6], +DI4[/43.9]	1 ~ 8 + LIMIT
+DI5[/43.C], +DI6[/43.F], +DI7[/44.2], +DI8[/44.5]	
-DI1[/43.1], -DI2[/43.4], -DI3[/43.7], -DI4[/43.A]	1 ~ 8 - LIMIT
-DI5[/43.D], -DI6[/44.0], -DI7[/44.3], -DI8[/44.6]	
Dd1[/43.2], Dd1[/43.5], Dd1[/43.8], Dd1[/43.B], Dd1[/43.E], Dd1[/44.1], Dd1[/44.4], Dd8[/44.7]	1 ~ 8

()

24) IP1~IP8[/44.8~/44.F] IN-POSITION ()

80P CLOSED LOOP 가 (P115) IN-POSITION
가 가 ON .

80P CLOSED LOOP 가
가 ON .

25) EcI0 ~ EchF[/45, /46]

MPG

HEX

.

9.2 MC

(PLC → MC) : PLC

9.2 MC

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Q00	OPC		DNC	MPG	STP	JOG	ORG	AUT	FIN	SYN		ESO	SP	ST	ERS	ESP
Q01		RT	R02	R01	OV8	OV4	OV2	OV1				AFL	MLK	BSK	SGL	DRN
Q02	A8-	A8+	A7-	A7+	A6-	A6+	A5-	A5+	A4-	A4+	A3-	A3+	A2-	A2+	A1-	A1+
Q03	Sov8	Sov4	Sov2	Sov1	SovE		MP2	MP1	H8	H7	H6	H5	H4	H3	H2	H1
Q04	SOF8	SOF7	SOF6	SOF5	SOF4	SOF3	SOF2	SOF1	DC8	DC7	DC6	DC5	DC4	DC3	DC2	DC1
Q05	-L8	+L8	-L7	+L7	-L6	+L6	-L5	+L5	-L4	+L4	-L3	+L3	-L2	+L2	-L1	+L1
Q06	PI1F	PI1E	PI1D	PI1C	PI1B	PI1A	PI19	PI18	PI17	PI16	PI15	PI14	PI13	PI12	PI11	PI10
Q07	Ph1F	Ph1E	Ph1D	Ph1C	Ph1B	Ph1A	Ph19	Ph18	Ph17	Ph16	Ph15	Ph14	Ph13	Ph12	Ph11	Ph10
Q08	PI2F	PI2E	PI2D	PI2C	PI2B	PI2A	PI29	PI28	PI27	PI26	PI25	PI24	PI23	PI22	PI21	PI20
Q09	Ph2F	Ph2E	Ph2D	Ph2C	Ph2B	Ph2A	Ph29	Ph28	Ph27	Ph26	Ph25	Ph24	Ph23	Ph22	Ph21	Ph20
Q10	PI3F	PI3E	PI3D	PI3C	PI3B	PI3A	PI39	PI38	PI37	PI36	PI35	PI34	PI33	PI32	PI31	PI30
Q11	Ph3F	Ph3E	Ph3D	Ph3C	Ph3B	Ph3A	Ph39	Ph38	Ph37	Ph36	Ph35	Ph34	Ph33	Ph32	Ph31	Ph30
Q12	PI4F	PI4E	PI4D	PI4C	PI4B	PI4A	PI49	PI48	PI47	PI46	PI45	PI44	PI43	PI42	PI41	PI40
Q13	Ph4F	Ph4E	Ph4D	Ph4C	Ph4B	Ph4A	Ph49	Ph48	Ph47	Ph46	Ph45	Ph44	Ph43	Ph42	Ph41	Ph40
Q14	PI5F	PI5E	PI5D	PI5C	PI5B	PI5A	PI59	PI58	PI57	PI56	PI55	PI54	PI53	PI52	PI51	PI50
Q15	Ph5F	Ph5E	Ph5D	Ph5C	Ph5B	Ph5A	Ph59	Ph58	Ph57	Ph56	Ph55	Ph54	Ph53	Ph52	Ph51	Ph50
Q16	PI6F	PI6E	PI6D	PI6C	PI6B	PI6A	PI69	PI68	PI67	PI66	PI65	PI64	PI63	PI62	PI61	PI60
Q17	Ph6F	Ph6E	Ph6D	Ph6C	Ph6B	Ph6A	Ph69	Ph68	Ph67	Ph66	Ph65	Ph64	Ph63	Ph62	Ph61	Ph60
Q18	PI7F	PI7E	PI7D	PI7C	PI7B	PI7A	PI79	PI78	PI77	PI76	PI75	PI74	PI73	PI72	PI71	PI70
Q19	Ph7F	Ph7E	Ph7D	Ph7C	Ph7B	Ph7A	Ph79	Ph78	Ph77	Ph76	Ph75	Ph74	Ph73	Ph72	Ph71	Ph70
Q20	PI8F	PI8E	PI8D	PI8C	PI8B	PI8A	PI89	PI88	PI87	PI86	PI85	PI84	PI83	PI82	PI81	PI80
Q21	Ph8F	Ph8E	Ph8D	Ph8C	Ph8B	Ph8A	Ph89	Ph88	Ph87	Ph86	Ph85	Ph84	Ph83	Ph82	Ph81	Ph80
Q22	FIF	FIE	FID	FIC	FIB	FIA	FI9	FI8	FI7	FI6	FI5	FI4	FI3	FI2	FI1	FI0
Q23	FhF	FhE	FhD	FhC	FhB	FhA	Fh9	Fh8	Fh7	Fh6	Fh5	Fh4	Fh3	Fh2	Fh1	Fh0
Q24	T1	T0			FwE	LrE	LE	PE	P7	P6	P5	P4	P3	P2	P1	P0
Q25	LF	LE	LD	LC	LB	LA	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0
Q26	LIF	LIE	LID	LIC	LIB	LIA	LI9	LI8	LI7	LI6	LI5	LI4	LI3	LI2	LI1	LI0
Q27	LhF	LhE	LhD	LhC	LhB	LhA	Lh9	Lh8	Lh7	Lh6	Lh5	Lh4	Lh3	Lh2	Lh1	Lh0
Q28	S8	S7	S6	S5	S4	S3	S2	S1	I8	I7	I6	I5	I4	I3	I2	I1
Q29	RIF	RIE	RID	RIC	RIB	RIA	RI9	RI8	RI7	RI6	RI5	RI4	RI3	RI2	RI1	RI0
Q30	RhF	RhE	RhD	RhC	RhB	RhA	Rh9	Rh8	Rh7	Rh6	Rh5	Rh4	Rh3	Rh2	Rh1	Rh0
Q31	SPE	SSE	SSD	SSC	SSB	SSA	SS9	SS8	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
Q32									ZS8	ZS7	ZS6	ZS5	ZS4	ZS3	ZS2	ZS1
Q33																
Q34																
Q35																
Q36																
Q37																
Q38																
Q39																
Q40																
Q41																
Q42																
Q43																

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Set	:	" 1 "	.	(LEVEL CHECK)
Momentary	:	" 0 " => " 1 "	.	(EDGE CHECK)
		LEVEL		2 Scan Time

- 1) ESP[Q0.0] EMERGENCY STOP () / Momentary
ERS[Q0.1] RESET () / Momentary

ESP[Q0.0] (0) → (1) EMERGENCY STOP .

ERS[Q0.1] (0) → (1) RESET
RESET RST[I0.2]가 ON .

- 2) OPC[Q0.F] () / Set

OPC[Q0.F] (1) "P23.0 OP CH" 가 .

- 3) ST[Q0.2] , STEP () / Momentary

AUTO[I0.8] , STEP[I0.B] MODE .

AUTO MODE 가 ST[Q0.2] (0) → (1) STL[I0.4] ,
MC
OP[I0.6] ON .

STEP MODE 가 ST[Q0.2] (0) → (1)

) "P23.0 OP CH"가 'Disable' .

- AUTO, STEP MODE가 .
- 가 ALARM . (AL[I0.3] ON)
- RESET . (RST[I0.2] ON)
- . (STL[I0.4] ON)

STL[I0.4] OFF .

-
- SP[Q0.3]가 (0) → (1) .
- RESET .
- SINGLE BLOCK 1 BLOCK .
- ALARM .
- MODE 가 .

4) SP[Q0.3] , STEP () / Momentary

AUTO[I0.8] , STEP[I0.8] MODE .

SP[Q0.3]가 (0) → (1)
STL[I0.4] OFF SPL[I0.5] ON .

) “P23.0 OP CH”가 ‘Disable’ .

5) ES0[Q0.4] OFF () / Set

ES0[Q0.4]가 (1) EMERGENCY STOP (ESP[Q0.0])가 (0) → (1)
SERVO ON SERVO BRAKE OFF .

6) [Q0.5]

7) SYN[Q0.6] () / Set

“P112.1 Q0.6 ”가 ‘Enable’ ,
SYN[Q0.6] (1) .

8) FIN[Q0.7] M CODE FINISH () / Set

MF[I2.7] ON FIN[Q0.7] (1) ,
MF[I2.7] OFF (0) .

9) AUTO[Q0.8] , ORG[Q0.9] , JOG[Q0.A] , STP[Q0.B] , MPG[Q0.C] , DNC[Q0.D]
MODE () / Momentary

MODE 가 (0) → (1) MODE 가 .
MODE (0) .

) “P23.0 OP CH”가 ‘Disable’ .

10) [Q0.E]

11) [Q0.F]

12) DRN[Q1.0] DRY RUN() / Set

MODE .

MODE (P31) .
가 (1) (P31) .

) “P23.0 OP CH”가 ‘Disable’ .

13) SGL[Q1.1] SINGLE BLOCK() / Set

MODE

가 (1) BLOCK
가 BLOCK

) “P23.0 OP CH”가 ‘Disable’

14) BCK[Q1.2] BLOCK SKIP() / Set

MODE

가 (1) MC ‘/’ ‘;’
BLOCK SKIP , BLOCK MC

) “P23.0 OP CH”가 ‘Disable’

15) MLK[Q1.3] MACHINE LOCK() / Set

가 (1)

가 MC Check

) “P23.0 OP CH”가 ‘Disable’

16) AFL[Q1.4] AUXILIARY FUNCTION LOCK() / Set

MODE

가 (1) M Code 가 M CODE FINISH (FIN)
MC Check

) “P23.0 OP CH”가 ‘Disable’

17) [Q1.5]

18) [Q1.6]

19) [Q1.7]

20) OV1[1.8], OV2[1.9], OV4[1.A], OV8[1.B] OVERRIDE () / Set

(AUTO MODE (G01,G02,G03) , JOG MODE) OVERRIDE

) “P23.0 OP CH”가 ‘Disable’ / P23.1 OV ENB 가 ENB ’

X: (0), 0: (1)

OV8[Q1.B]	OV4[Q1.A]	OV2[Q1.9]	OV1[Q1.8]	OVERRIDE
X	X	X	X	0 %
X	X	X	0	10 %
X	X	0	X	20 %

X	X	0	0	30 %
X	0	X	X	40 %
X	0	X	0	50 %
X	0	0	X	60 %
X	0	0	0	70 %
0	X	X	X	80 %
0	X	X	0	90 %
0	X	0	X	100 %
0	X	0	0	110 %
0	0	X	X	120 %
0	0	X	0	130 %
0	0	0	X	140 %
0	0	0	0	150 %

21) ROV2[Q1.D], ROV1[[Q1.C] OVERRIDE ()/Set

(AUTO MODE (G00)) OVERRIDE .

) “P23.0 OP CH”가 ‘Disable’ / P23.2 ROV ENB 가 ENB ’ .

R02[Q1.D]	R01[Q1.C]	OVERRIDE
X	X	0 %
X	0	25 %
0	X	50 %
0	0	100 %

X: (0), 0: (1)

22) RT[Q1.E] () / Set

JOG[I0.A], ORG[I0.G] MODE (1) (P35) JOG

) “P23.0 OP CH”가 ‘Disable’ .

23) [Q1.F]

24)

A1+[Q2.0], A1-[Q2.1], A2+[Q2.2], A2-[Q2.3], A3+[Q2.4], A3-[Q2.5], A4+[Q2.6], A4-[Q2.7],
A5+[Q2.8], A5-[Q2.9], A6+[Q2.A], A6-[Q2.B], A7+[Q2.C], A7-[Q2.D], A8+[Q2.E], A8-[Q2.F]
, () / Set

JOG[I0.A], ORG[I0.G] MODE .

) “P23.0 OP CH”가 ‘Disable’ .

25) H1[Q3.0], H2[Q3.1], H3[Q3.2], H4[Q3.3], H5[Q3.4], H6[Q3.5], H7[Q3.6], H8[Q3.7]

MPG () / Set

MPG[I0.C] MODE

) “P23.0 OP CH”가 ‘Disable’ .

26) MP1[Q3.8], MP2[Q3.9] MPG () / Set

) “P23.0 OP CH”가 ‘Disable’ .

MP2[Q3.9]	MP1[Q3.8]	
X	X	* 1
X	0	*10
0	X	*100
0	0	*100

X: (0), 0: (1)

27) [Q3.A]

28) SovE[Q3.B], Sov1[Q3.C], Sov2[Q3.D], Sov4[Q3.E], Sov8[Q3.F]

OVERRIDE () / Set

SovE[Q3.B]가 (1)

Sov1[Q3.C], Sov2[Q3.D], Sov4[Q3.E], Sov8[Q3.F]

OVERRIDE 가

X: (0), 0: (1)

Sov8[Q3.F]	ov4[Q3.E]	Sov2[Q3.D]	Sov1[Q3.C]	OVERRIDE
X	X	X	X	0 %
X	X	X	0	10 %
X	X	0	X	20 %
X	X	0	0	30 %
X	0	X	X	40 %
X	0	X	0	50 %
X	0	0	X	60 %
X	0	0	0	70 %
0	X	X	X	80 %
0	X	X	0	90 %
0	X	0	X	100 %
0	X	0	0	110 %
0	0	X	X	120 %
0	0	X	0	130 %
0	0	0	X	140 %
0	0	0	0	150 %

% : Q31.E ~ Q31.F / : P51 ~ P53 / : 2

29) DC1[Q4.0], DC2[Q4.1], DC3[Q4.2], DC4[Q4.3],
DC5[Q4.4], DC6[Q4.5], DC7[Q4.6], DC8[Q4.7]

() / Set

“P21.2 Switch” B (NORMAL CLOSE) A (NORMAL OPEN)

) “P21.1 / ”가 ‘Enable’, “P25 Dog Choice”가 ‘PLC’ .

30) SVOF1 ~ SVOF8[Q4.8~Q4.F] SERVO OFF () / Momentary

SVOF1 ~ SVOF8[Q4.8 ~ Q4.F] (0) → (1) SERVO OFF ,
(1) → (0) SERVO ON .

31)

+L1[Q5.0], -L1[Q5.1], +L2[Q5.2], -L2[Q5.3], +L3[Q5.4], -L3[Q5.5], +L4[Q5.6], -L4[Q5.7],
+L5[Q5.8], -L5[Q5.9], +L6[Q5.A], -L6[Q5.B], +L7[Q5.C], -L7[Q5.D], +L8[Q5.E], -L8[Q5.F]
Limit Switch () / Set

“P21.3 + Limit Switch”, “P21.4 - Limit Switch” B (NORMAL CLOSE)
A (NORMAL OPEN)

) “P21.3 + Limit Switch”, “P21.4 - Limit Switch” 가 ‘
“P24 Limit Choice” 가 ‘PLC’

32)

PI10 ~ Ph1F[Q6, Q7]	1	STEP MODE	/ Set
PI20 ~ Ph2F[Q8, Q9]	2	STEP MODE	/ Set
PI30 ~ Ph3F[Q10, Q11]	3	STEP MODE	/ Set
PI40 ~ Ph4F[Q12, Q13]	4	STEP MODE	/ Set
PI50 ~ Ph5F[Q14, Q15]	5	STEP MODE	/ Set
PI60 ~ Ph6F[Q16, Q17]	6	STEP MODE	/ Set
PI70 ~ Ph7F[Q18, Q19]	7	STEP MODE	/ Set
PI80 ~ Ph8F[Q20, Q21]	8	STEP MODE	/ Set

STEP[10.B] MODE HEX

33) FI0 ~ FhF[Q22, Q23] STEP MODE / Set

STEP[10.B] MODE HEX

34) P0 ~ P7[Q24.0~Q24.7] / Set
PE[Q24.8] Enable / Momentary

AUTO[10.8] MODE HEX
PE[Q24.8]가 (0) → (1)

35) LE[Q24.9] L / Momentary

L LE[Q24.9]가 (0) → (1)

36) LrE(L Read Enable[Q24.A]) L READ / Momentary

L0 ~ LF[Q25]: L HEX
L READ LrE(L Read Enable[Q24.A])가 (0) → (1)
MC->PLC L10 ~ LhF[141, 142] HEX MC->PLC LrE(L Read
End[123.A]) 가 ON

37) [Q24.B]

38) [Q24.C]

39) [Q24.D]

40) T0[Q24.E], T1[Q24.F] STEP MODE TYPE / Set

T1[Q24.F]	T0[Q24.E]	TYPE
X	X	G00
X	0	G01
0	X	G02
0	0	G03

X: (0), 0: (1)

I1~I8[Q28.0~Q28.7]	() 가 ()
S1~S8[Q28.8~Q28.F]	() .
R10~RhF[Q29, Q30]	TYPE HEX .

41) L0 ~ LF[Q25] L / Set : L HEX .

L10 ~ LhF[Q26, Q27] L / Set : L HEX .

L LE[Q24.9]가 (0) → (1)

42) I1~I8[Q28.0~Q28.7] Q24.E/Q24.F STEP MODE TYPE / Set

43) S1~S8[Q28.8~Q28.F] Q24.E/Q24.F STEP MODE TYPE / Set

44) R10~RhF[Q29, Q30] Q24.E/Q24.F STEP MODE TYPE / Set

45) SPE[Q31.F], SS0 ~ SSE[Q31.0~Q31.E] () / Set

SPE[Q31.F] (1) 가 SS0 ~ SSE[Q31.0~Q31.E]

% : Q3.B ~ Q3.F / : P51 ~ P53 / : 2

46) ZS1~ZS8[Q32.0~Q32.7] () / Momentary

ZS1~ZS8[Q32.0~Q32.7]가 (0) → (1) 가 L (40~47)

9.3

1) MCS-80

9.3 MCS-80 /

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
X0.F~X0.0	AXIS 3/4						AXIS 1/2									
X1.F~X1.0			AXIS 5/6													
X2.F~X2.0	x	x	x	x	x	x	x	x	AXIS 7/8							
X3.F~X3.0	I/O (32)															
X4.F~X4.0																
X5.F~X5.0																
Y0.F~Y0.0	AXIS 5/6				AXIS 3/4						AXIS 1/2					
Y1.F~Y1.0	Axis I/O 1,2 Brake								AXIS 4							
Y2.F~Y2.0	I/O (24)															
Y3.F~Y3.0	x	x	x	x	x	x	x	x								
Y4.F~Y4.0																
Y5.F~Y5.0																
I00.F~I00.0	MC (MC -> PLC)															
.																
.																
I99.F~I99.0	MC (PLC -> MC)															
Q00.F~Q00.0																
.																
.																
.																
Q99.F~Q99.0																
F0.F~F0.0																
F1.F~F1.0																
.																
F8.F~F8.0																
F9.F~F9.0																
T0.F~T0.0																
T1.F~T1.0																
C0.F~C0.0																
C1.F~C1.0																
M0.F~M0.0																
...																
M98.F~M98.0																
M99.F~M99.0																

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
D0																
...																
D383																
D384																
...																
D415																
D416																
...																
D447																
D448																
...																
D479																
D480																
...																
D511																
X1.0.F~X1.0.0	(1 (<- 1))															
...																
X1.4.F~X1.4.0																
Y1.0.F~Y1.0.0	(1 (-> 1))															
...																
Y1.4.F~Y1.4.0																
X2.0.F~X2.0.0																
...																
Y63.4.F~Y63.4.0																

(1) : X0.0 ~ X5.F

- AXIS : X0.0 ~ X2.7

X0.0 ~ X2.7	MCS-80 AXIS

- I/O : X3.0 ~ X4.F

X3.0 ~ X4.F	MCS-80 I/O

* AXIS (:)

-

가 .

AIXS					
AXIS-1			AXIS-2		
Connect			Connect		
IN0	X0.0	Servo Ready-1	IN10	X0.A	Servo Ready-3
IN1	X0.1	Servo Ready-2	IN11	X0.B	Servo Ready-4
IN2	X0.2	Servo Alarm-1	IN12	X0.C	Servo Alarm-3
IN3	X0.3	Servo Alarm-2	IN13	X0.D	Servo Alarm-4
IN4	X0.4		IN14	X0.E	
IN5	X0.5		IN15	X0.F	
IN6	X0.6		IN16	X1.0	
IN7	X0.7		IN17	X1.1	
IN8	X0.8		IN18	X1.2	
IN9	X0.9		IN19	X1.3	

AIXS					
AXIS-3			AXIS-4		
Connect			Connect		
IN0	X1.4	Servo Ready-5	IN10	X1.E	Servo Ready-7
IN1	X1.5	Servo Ready-6	IN11	X1.F	Servo Ready-8
IN2	X1.6	Servo Alarm-5	IN12	X2.0	Servo Alarm-7
IN3	X1.7	Servo Alarm-6	IN13	X2.1	Servo Alarm-8
IN4	X1.8		IN14	X2.2	
IN5	X1.9		IN15	X2.3	
IN6	X1.A		IN16	X2.4	
IN7	X1.B		IN17	X2.5	
IN8	X1.C		IN18	X2.6	
IN9	X1.D		IN19	X2.7	

(2) : Y0.0 ~ Y5.F

- AXIS : Y0.0 ~ Y1.7

Y0.0~Y1.7	MCS-80 AXIS
Y1.8~Y1.F	()

- I/O : Y2.0 ~ Y3.7

Y2.0~Y2.7	MCS-80 I/O
Y2.8~Y2.F	()

* AXIS (:)

- 가 .

AXIS					
AXIS-1			AXIS-2		
Connect			Connect		
OUT0	Y0.0	Servo 0n-1	OUT6	Y0.6	Servo 0n-3
OUT1	Y0.1	Servo 0n-2	OUT7	Y0.7	Servo 0n-4
OUT2	Y0.2		OUT8	Y0.8	
OUT3	Y0.3		OUT9	Y0.9	
OUT4	Y0.4		OUT10	Y0.A	
OUT5	Y0.5		OUT11	Y0.B	

AIXS					
AXIS-3			AXIS-4		
Connect			Connect		
OUT0	Y0.C	Servo 0n-5	OUT6	Y1.2	Servo 0n-7
OUT1	Y0.D	Servo 0n-6	OUT7	Y1.3	Servo 0n-8
OUT2	Y0.E		OUT8	Y1.4	
OUT3	Y0.F		OUT9	Y1.5	
OUT4	Y1.0		OUT10	Y1.6	
OUT5	Y1.1		OUT11	Y1.7	

(3) MC (MC -> PLC) : 100.0 ~ 199.F

- : “ 9 /9.1 MC (MC→PLC) ”

(4) MC (PLC -> MC) : Q00.0 ~ Q99.F

- : “ 9 /9.2 MC (PLC→MC) ”

(5) : F0.0 ~ F9.F

- : F0.0 ~ F1.F

F0.0	ON	F1.0	Carry
F0.1	OFF	F1.1	
F0.2	ON	F1.2	
F0.3	OFF	F1.3	
F0.4		F1.4	
F0.5	10ms	F1.5	
F0.6	50ms	F1.6	- NVRAM
F0.7	100ms	F1.7	- NVRAM
F0.8	200ms	F1.8	10ms
F0.9	1s	F1.9	10ms
F0.A	10s	F1.A	4ms
F0.B	60s	F1.B	4ms
F0.C		F1.C	
F0.D		F1.D	
F0.E		F1.E	Watch-Dog
F0.F		F1.F	Watch-Dog

- : F2.0 ~ F9.F

F2.0~F2.F	PLC	(Peak)	HEX	(mSec)
F3.0~F3.F	PLC	HEX			
F4.0~F4.F	Scan PLC	(Peak)	HEX	(mSec)
F5.0~F5.F	Scan PLC	HEX			
F6.0~F6.F	HEX				
F7.0~F7.F	HEX				
F8.0~F8.F	HEX				
F9.0~F9.F	HEX				

(6) : T0.0 ~ T1.F

- PLC TMR, TON, TOFF 0 ~ TMR, TON, TOFF 31 31

(7) : C0.0 ~ C1.F

- PLC CTR 0 ~ CTR 31 31

(8) : M00.0 ~ M99.F

- : M00.0 ~ M99.F, .

(9) : D000.0 ~ D383.F

- : D000.0 ~ D383.F, .

- , : D384.0 ~ D511.F, / ,

- .

(10) : D384 ~ D415

- PLC TMR, TON, TOFF 0 ~ TMR, TON, TOFF 31 31

- PLC , . ()

- MSW-MCS S/W 가 .

(11) : D416 ~ D447

- PLC TMR, TON, TOFF 0 ~ TMR, TON, TOFF 31

31 ()

(12) : D448 ~ D479

- PLC CTR 0 ~ CTR 31 31

- PLC . ()

- MSW-MCS S/W 가 .

(13) : D480 ~ D511

- PLC CTR 0 ~ CTR 31 31 ()

(14) : X1.0.0 ~ X63.4.F

(15) : Y1.0.0 ~ Y63.4.F

9.4

9.6 MCS-80

	MODBUS	MELSEC-UC24/C24	LG	OMRON	
X0.F~X0.0	10001~10096(bit)	X0000~X005F(C24)	P0~P5(MK)	C10 0000 00	
...	30001~30006(word)	X000000~X00005F(UC24)	IW0~IW5(GM)	~	
X5.F~X5.0				C10 0005 15	
Y0.F~Y0.0	1~96(bit)	Y0000~Y005F(C24)	P6~P11(MK)	C10 0100 00	
...	40001~40006(word)	Y000000~Y00005F(UC24)	QW0~QW5(GM)	~	
Y5.F~Y5.0				C10 0105 15	
I00.F~I00.0	10101~11700(bit)	R0000~R0099(C24-word)	MW100~	C10 0200 00 ~	MC (MC -> PLC)
...	40101~40200(word)	R000000~R000099(UC24-word)	MW199(MK, GM)	C10 0299 15	
I99.F~I99.0		R0000~R1599(C24-bit)			
		R000000~R001599(UC24-bit)			
Q00.F~Q00.0	101~1700(bit)	L0000~L1599(C24)	MW200~	C10 0300 00 ~	MC (PLC -> MC)
...	40201~40300(word)	L000000~L001599(UC24)	MW299(MK, GM)	C10 0399 15	
Q99.F~Q99.0					
F0.F~F0.0	1701~1860(bit)	F0000~F0159(C24)		C10 0400 00 ~	
...	40301~40310(word)	F000000~F000159(UC24)		C10 0409 15	
F9.F~F9.0					
T0.F~T0.0	1901~1932(bit)	TC0000~TC0031(C24)	MW300~	C10 0500 00 ~	
T1.F~T1.0	40401~40402(word)	TC000000~TC000031(UC24)	MW301(MK, GM)	C10 0501 15	
C0.F~C0.0	2001~2032(bit)	CC0000~CC0031(C24)	MW302~	C10 0600 00 ~	
C1.F~C1.0	40501~40502(word)	CC000000~CC000031(UC24)	MW302(MK, GM)	C10 0601 15	
M00.F~M00.0	2101~3700(bit)	M0000~M1599(C24)	MW0~	C10 0800 00 ~	
...	40601~40700(word)	M000000~M001599(UC24)	MW99(MK, GM)	C10 0899 15	
M99.F~M99.0					
D000		D0000~D0383(C24-word)	D000~	C10 1000 00 ~	
...	40701~41084(word)	D000000~D000383(UC24-word)	D383(MK)	C10 1383 15	
D383		D0000~D6143(C24-bit)	MW400~		
		D000000~D006143(UC24-bit)	MW783(GM)		
D384		D0384~D0415(C24-word)	D384~	C10 1384 00 ~	
...	41085~41116(word)	D000384~D000415(UC24-word)	D415(MK)	C10 1415 15	
D415		D6144~D6655(C24-bit)	MW738~		
		D006144~D006625(UC24-bit)	MW815(GM)		
D416		D0416~D0447(C24-word)	D416~	C10 1416 00 ~	
...	41117~41148(word)	D000416~D000447(UC24-word)	D447(MK)	C10 1447 15	
D447		D6656~D7167(C24-bit)	MW816~		
		D006656~D007167(UC24-bit)	MW847(GM)		
D448		D0448~D0479(C24-word)	D448~	C10 1448 00 ~	
...	41149~41180(word)	D000448~D000479(UC24-word)	D479(MK)	C10 1479 15	
D479		D7168~D7679(C24-bit)	MW848~		
		D007168~D007679(UC24-bit)	MW879(GM)		
D480		D0480~D0511(C24-word)	D480~	C10 1480 00 ~	
...	41181~41212(word)	D000480~D000511(UC24-word)	D511(MK)	C10 1511 15	
D511		D7680~D8191(C24-bit)	MW880~		
		D007680~D008191(UC24-bit)	MW911(GM)		
X1.0.F~X1.0.0	10101~14132(bit-X)	B0000~B8063(C24)		C10 1800 00 ~	
...	4001~8032(bit-Y)	B000000~B008063(UC24)		C10 2429 15	
Y63.4.F~Y63.4.0	42001~42504(word)				

9.7 MCS-80

MC

L (32Bit)	MELSEC-UC24/C24	LG	
L0	W0000 ~ W3E7F(C24) W000000 ~ W003E7F(UC24)	L0000 ~ L9999(MK) MW1000 ~ MW9999(GK)	MC
...			
L7999			

- L

	MELSEC-UC24/C24		
L (32Bit)			
L0	W1-W0	W0	32Bits
L1	W3-W2	W2	
L2	W5-W4	W4	
...	
L7997	W3E7B-W3E7A	W3E7A	
L7998	W3E7D-W3E7C	W3E7C	
L7999	W3E7F-W3E7E	W3E7E	

9.5 MELSEC

2

MMI

- 1) : 9.1 MC
- (1) : I01.8 (MR1)~I01.9 (MR2)
- (2) : I00.3 (AL)
: I24.F ~ I24.0 (AF~A0 (16Bits))

100	SERVO NOT READY	SERVO READY 가 .
101	SERVO ALARM	SERVO ALARM 가 .
106	FOLLOWING ERROR	가 (P71:) .

- 2) RUN/STOP : 9.2 MC
- (1) STEP → PLC : Q00.B (STEP)
- (2) SET : Q23.F~Q22.0 (FhF~FI0 (32Bits))
: Q28.8 (S1)
: 0~24000 (mm/min)
- (3) RUN/STOP – A1+(or A1-) : Q02.0 (A1+) (or Q02.1(A1-))
- (4) RESET - ERS : MOMENTARY
: Q00.1 (Off → On → Off)

3) MESEC-UC24

(AnA/AnU)

(1)

- : I01.8(MR1)~I01.9(MR2)

		PC					SUM
ENQ	01	FF	QR	0	R000001	01	94
05	3031	4646	5152	30	52303030303031	3031	3934

** SUM (94) <= 94 <= 394 <= 30+31 +46+46 +51+52 +30 +52+30+30+30+30+30+31 +30+31

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

** SUM (??) <= ?? <= x?? <= 30+31 +46+46 +D(3)+D(2)+D(1)+D(0) +03

- : I00.3(AL)

		PC					SUM
ENQ	01	FF	QR	0	R000000	01	93
05	3031	4646	5152	30	52303030303030	3031	3933

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

- : I24.F~I24.0(AF~A0 (16Bits))

		PC					SUM
ENQ	01	FF	QR	0	R000024	01	99
05	3031	4646	5152	30	52303030303234	3031	3939

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

(2)

RUN/STOP

- STEP : Q00.B (STEP) On → PLC
 LOAD 1
 OUT Q00.B

- : Q23.F~Q22.0 (FhF~F10 (32Bits))

		PC						SUM
ENQ	01	FF	QW	0	L000352	02	8Byte	??
05	3031	4646	5157	30	4C303030333532	3032	D(3)D(2)D(1)D(0) D(7)D(6)D(5)D(4)	^^

		PC
ACK	01	FF
06	3031	4646

- : Q28.8 (S1) On

		PC						SUM
ENQ	01	FF	JW	0	L000456	01	1	CB
05	3031	4646	5157	30	4C303030343536	3031	31	4342

		PC
ACK	01	FF
06	3031	4646

RUN/STOP - + /

- RUN : Q02.0 (A1+) On

		PC						SUM
ENQ	01	FF	JW	0	L000032	01	1	C1
05	3031	4646	4A57	30	4C303030303332	3031	31	4331

		PC
ACK	01	FF
06	3031	4646

- STOP : Q02.0 (A1+) Off

		PC						SUM
--	--	----	--	--	--	--	--	-----

ENQ	01	FF	JW	0	L000032	01	0	C0
05	3031	4646	4A57	30	4C303030303332	3031	30	4330

-

		PC
ACK	01	FF
06	3031	4646

RESET -

- ERS : Q00.1 (ERS) On

		PC						SUM
ENQ	01	FF	JW	0	L000001	01	1	BD
05	3031	4646	4A57	30	4C303030303031	3031	31	4244

		PC
ACK	01	FF
06	3031	4646

- ERS : Q00.1 (ERS) Off

		PC						SUM
ENQ	01	FF	JW	0	L000001	01	0	BC
05	3031	4646	4A57	30	4C303030303031	3031	30	4243

		PC
ACK	01	FF
06	3031	4646

4) MESEC-C24

(AnN/AnS/A0J2)

(1)

- : I01.8 (MR1)~I01.9 (MR2)

		PC					SUM
ENQ	01	FF	WR	0	R0001	01	3A
05	3031	4646	5152	30	523030303	3031	3934

** SUM (3A) <= 3A <= 33A <= 30+31 +46+46 +57+52 +30 +52+30+30+30+31 +30+31

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

** SUM (??) <= ?? <= x?? <= 30+31 +46+46 +D(3)+D(2)+D(1)+D(0) +03

- : I00.3 (AL)

		PC					SUM
ENQ	01	FF	WR	0	R0000	01	39
05	3031	4646	5752	30	5230303030	3031	3933

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

- : I24.F~I24.0(AF~A0 (16Bits))

		PC					SUM
ENQ	01	FF	WR	0	R0024	01	3F
05	3031	4646	5752	30	5230303234	3031	3446

		PC					SUM
STX	01	FF	4Byte			ETX	??
02	3031	4646	D(3)D(2)D(1)D(0)			03	^^

(2)

RUN/STOP

- STEP : Q00.B (STEP) On → PLC
 LOAD 1
 OUT Q00.B

- : Q23.F~Q22.0 (FhF~F10 (32Bits))

		PC						SUM
ENQ	01	FF	WW	0	L0352	02	8Byte	??
05	3031	4646	5757	30	4C30333532	3032	D(3)D(2)D(1)D(0) D(7)D(6)D(5)D(4)	^^

		PC
ACK	01	FF
06	3031	4646

- : Q28.8 (S1) On

		PC						SUM
ENQ	01	FF	BW	0	L0456	01	1	63
05	3031	4646	4257	30	4C30343536	3031	31	3633

		PC
ACK	01	FF
06	3031	4646

RUN/STOP - + /

- RUN : Q02.0 (A1+) On

		PC						SUM
ENQ	01	FF	BW	0	L0032	01	1	59
05	3031	4646	4257	30	4C30303332	3031	31	3539

		PC
ACK	01	FF
06	3031	4646

- STOP : Q02.0 (A1+) Off

-

		PC						SUM
ENQ	01	FF	BW	0	L0032	01	0	58
05	3031	4646	4257	30	4C30303332	3031	30	3538

-

		PC
ACK	01	FF
06	3031	4646

RESET -

- ERS : Q00.1 (ERS) On

-

		PC						SUM
ENQ	01	FF	BW	0	L0001	01	1	55
05	3031	4646	4257	30	4C30303031	3031	31	3535

-

		PC
ACK	01	FF
06	3031	4646

- ERS : Q00.1 (ERS) Off

-

		PC						SUM
ENQ	01	FF	BW	0	L0001	01	0	54
05	3031	4646	4257	30	4C30303031	3031	30	3534

-

		PC
ACK	01	FF
06	3031	4646

